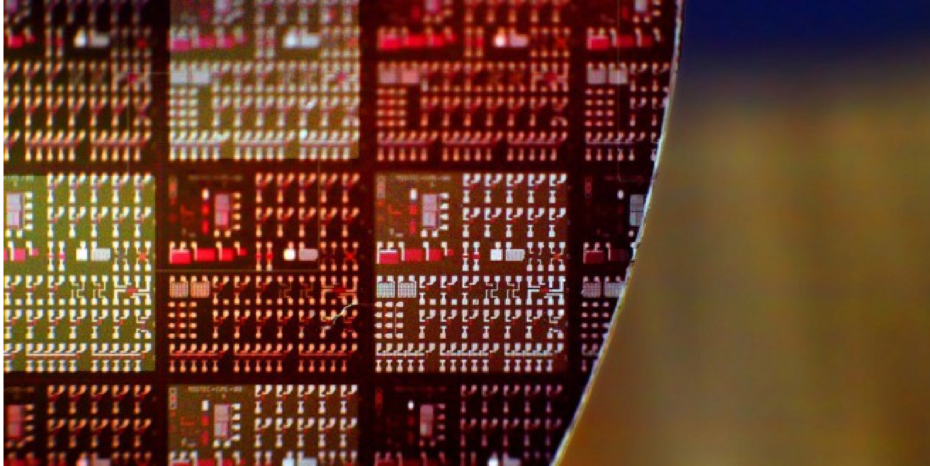

REDUCING IC MANUFACTURING COST WHILE ENHANCING IOT SECURITY

By some estimates, lithography now accounts for 50% of wafer cost. Since 2007 when 193nm immersion (193i) lithography reached its 80nm resolution limit, semiconductor lithography has undergone a series of seismic shifts:

At 28nm node and below, leading IC companies have adopted unidirectional (1D) design layout style with "Lines and Cuts" to facilitate manufacture of advanced IC designs.

- At 20nm node and below, leading fabs are deploying "pitch splitting" (also called "pitch division") using advanced deposition and etch technologies to achieve line-pitch resolution much smaller than the 80nm limit.
- At 14nm node and below, printing line-cuts and contact/via holes with 193i requires "multiple patterning" with multiple masks and mask steps.

Today, 193i multi-patterning is driving up costs while increasing overlay errors and cycle time. The severity of these challenges has no parallel in the history of IC manufacturing. And there is no optical solution to mitigate the soaring costs and negative impact on cycle times and yield. In addition, the burgeoning Internet of Things (IoT) market is imposing new demands on IC makers to reduce prototyping cost and enhance IoT security.

There are viable solutions to these challenges. And the solutions center on CEBL – the relatively new industry acronym for Complementary E-Beam Lithography.

What exactly is CEBL?
CEBL is a new class of electron-beam lithography (EBL). It's well known that EBL needs no masks and affords high resolution, and is an essential tool in the R&D lab. However, its low throughput has kept it out of production environments. Just as IC manufacturing has advanced, so also has electron-beam technology. With 1D layout widely adopted, CEBL provides a compelling solution to reduce multi-patterning cost and cycle time.

IC layers that require 193i multi-patterning of cuts or holes are known as "critical layers" and are the most demanding and costly. Take a critical layer with 1D lines-and-cuts layout, and two lithography technologies, namely, 193i and CEBL. Let 193i print the "lines", doing what it does best; then let e-beam write the "cuts" of the lines directly on wafer without masks (Fig. 1).

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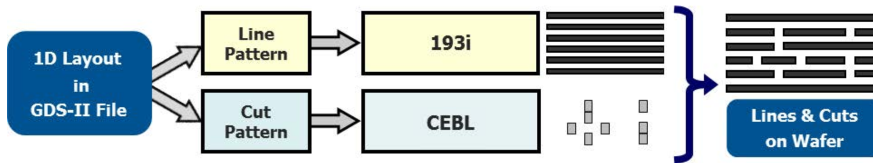

Fig. 1. CEBL complements 193i in patterning a critical layer. Source: Tela Innovations, Multibeam.

The role of CEBL is to pattern line-cuts and holes to complement and extend 193i lithography. In other words, CEBL writes cut patterns in polysilicon (or other materials) lines in the gate layer, metal lines in the interconnect layers, and fins in finFET devices; and CEBL patterns holes in contact and via layers. All these are critical mask layers in BEOL.

How CEBL reduces manufacturing cost and cycle time
193i multi-patterning, a direct consequence of 193i resolution limit, is a major driver of escalating cost. At 20nm node, for example, a set of masks costs $5 million, and the cost continues to mount unabated. Here are the detrimental effects of multi-patterning:

- At 14nm node, there are at least 14 design layers for which single patterning would not work, thus requiring 27 critical mask layers. At 10nm node, the number of critical mask layers jumps to 42 or more.
- As critical layers soar, so do masks per set. While 44 masks are needed to process 45nm node ICs, 68 masks are required at 14/16nm. While patterning steps (i.e., mask steps) grow proportionately, the number and cost of 193i tools rise as well.
- Multi-patterning also reduces the error budget for each critical mask layer. In triple patterning, for instance, each critical layer would have only one-third of the error budget for the layer with single patterning. This threatens or impacts yield due to increased overlay errors.
- Cycle time has stretched longer due to increased process complexity, and multi-patterning has compounded the problem. Not long ago, it took less than 1 day per mask layer in production; now it's edging up toward 2 days. More mask steps and more time for each mask layer means fewer wafers are produced in a given period of time.

While pitch splitting adds process steps to improve resolution, the use of deposition/etch to achieve this benefit needs no masks. Moreover, these sequential steps are amenable to process integration to reduce cycle time. In the end, 193i multi-patterning is the primary reason why lithography cost runs high and cycle time gets longer.

CEBL directly patterns cuts/holes to eliminate the need for costly masks associated with 193i multi-patterning. In addition to lowering production cost, CEBL reduces cycle time and improves yield.

How CEBL differs from other e-beam systems
While all electrons are the same, all EBL systems are not created equal. Indeed, CEBL is far different from other e-beam maskless lithography called ML or ML2.

ML systems are designed to pattern random 2D layouts for any and all layers on wafer, aspiring to be the next-generation lithography (NGL) replacing optical lithography. Typically, ML systems employ a single e-beam column, writing pixel by pixel, scanning the whole wafer. Empirical data collected over some 30 years and published in 1999 show that such EBL systems suffer from rapid deterioration in throughput as resolution improves. Even if the single e-beam is split into many thousands of beamlets, ML systems are too slow for wafer production.

As a dedicated complementary tool, CEBL is not NGL seeking to supplant 193i. And CEBL deployment requires no new infrastructure. In fact, it helps preserve the multibillion-dollar investments in optical lithography infrastructure while extending the productive use of 193i.

CEBL cost-efficiency in high-volume manufacturing
Production-worthy CEBL offers a remarkably fresh approach (Table 1):

- E-beam columns are made very small so that up to 100 can be deployed in a modular array. Multi-column parallel writing is faster than single-column writing used in the past.
- Electrons write shots, not pixel by pixel, to reduce write time.
- Electrons write cut and hole patterns in critical layers, not 2D layout in all layers.

	Complementary EB Lithography (CEBL)	EB Maskless Lithography (ML or ML2)

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Number of EB Columns	100	1
How Electrons Write	Shots	Pixels

Table 1. CEBL is fundamentally different from ML or ML2 e-beam lithography systems

Typically, cut patterns in 1D layout occupy 5% of the wafer in the aggregate. With the right approach, electrons are directed to expose cut features, skipping 95% of the wafer where there are no cuts, greatly boosting write speed.

A single CEBL module writes 5 wafers per hour, good for low-volume production and prototyping. Each CEBL module compares in size to a plasma etch module. For high-volume manufacturing, multiple identical writing modules are integrated to become a cost-efficient cluster tool.

How CEBL can reduce IoT prototyping cost and enhance security
Many believe the Internet of Things (IoT) will be a major growth driver for the semiconductor industry. Some predictions put the number of digitally connected IoT devices at tens of billions in five years.

As IoT deployment unfolds, two major concerns have arisen: device development cost and embedded security. CEBL not only helps to lower cost but is an ideal solution for enhancing IoT security. Here is how it works.

Device development cost
Early IoT applications leverage mature process nodes such as 90nm, 45nm and 28nm, which are produced with no multi-patterning. However, the diversity of IoT applications demands a large variety of devices. CEBL enables rapid low-cost prototyping.

- Mask cost. CEBL patterning 1D lines-and-cuts needs only “line” masks, no “cut” masks. CEBL patterning of holes needs no mask at all. Prototyping cost is dramatically reduced.
- Respin turnaround. Design changes are made through modifications of the design database of “cuts” or “holes”, no need for a new set of masks. Respin is fast.

As the IoT market evolves, smaller nodes may be required for certain applications. Advanced IoT devices will enjoy lower production cost afforded by CEBL in the same manner as other advanced ICs.

Chip-embedded security
Experts have warned that the billions of interconnected IoT devices present unprecedented vulnerability to security attacks. The defense against cyberattack, experts agree, should involve not only software but also embedded security in each device.

CEBL systems can embed three types of chip-specific security cost-efficiently during production via the design database for CEBL patterning.

- Individual chip ID. Embedded individual ID is the best defense against counterfeiting since it cannot be modified once embedded.
- Encryption data. Embedded “private key” encryption ensures secure authentication and offers the best defense against device hacking.
- Internet protocol (IP). Hardware-embedded IP address is truly non-volatile.

Chip-specific data can be inserted whether the design layout is 1D lines-&-cuts or conventional 2D. For example, suppose the security data are to be written in the Via-3 layer. CEBL needs only the design database for that layer to include the specific “security pattern”, regardless of layout style.

The ability to write chip-specific data is unique to CEBL – a capability not available with 193i optical or EUV lithography. Additional applications beyond those described here are certain to follow. Significantly, there is no impact on writing time when including chip-specific data.

Conclusion
CEBL is designed to pattern cuts and holes in critical layers to extend the productive use of 193i systems and infrastructure while substantially reducing production cost and cycle time. For IoT devices, CEBL offers a timely solution for rapid prototyping at low cost while preventing counterfeiting and hacking with chip-specific security data embedded in the device.

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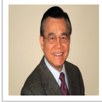
ABOUT DR. DAVID LAM



David K. Lam is Chairman of Multibeam Corporation, a leading developer of Complementary E-Beam Lithography (CEBL) systems based in Santa Clara, California. Lam is the founder and first CEO of Lam Research. Multibeam's CEBL is designed to pattern cuts and holes in critical layers for advanced-node manufacturing. CEBL extends the productive use of optical lithography systems and infrastructure while replacing multi-patterning and reducing cost and cycle time. Multibeam recently disclosed its proprietary Directed Electron Writing (DEW) technology, which embeds hardware security into IoT ("Internet of Things") devices. DEW inserts chip-specific information into each IoT including chip ID, communication address, and private key encryption. The on-chip security, implemented during production, is rapid and cost-efficient regardless of design layout style or the maturity of the process node. DEW-enabled security ensures secure authentication, protects against IC counterfeiting, enables supply chain traceability, and facilitates safe Internet communication. It complements software security and bolsters cyber-defense of IoT devices connected to homes, automobiles, offices, and facilities, which may in turn link to critical infrastructures such as power grid, nuclear reactors, and wafer fabs. Dr. Lam earned his master's and doctoral degrees in chemical engineering from M.I.T. and a bachelor's degree in engineering physics from the University of Toronto. Widely recognized as a contributor to the growth of Silicon Valley's semiconductor industry, he was inducted into the Silicon Valley Engineering Hall of Fame in 2013.

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